Hall Ticket Number:

Code No. : 14452 AS O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.C.E.) IV-Semester Advanced Supplementary Examinations, September-2022

Digital System Design

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	State De Morgan's theorems.	2	1	1	1
2.	Convert $(23.75)_{10}$ to base 2.	2	2	1	2
3.	Write the truth table of a full sub tractor.	2	1	2	1
4.	List any two applications of Encoders.	2	1	2	1
5.	Explain the differences between combinational and sequential circuits	2	2	3	1
6.	Recall the state table of a JK flip flop	2	1	3	1
7.	Give examples for any two data types in Verilog HDL	2	2	4	1
8.	Write the syntax of conditional operator in Verilog HDL.	2	1	4	1
9.	Explain the difference between Moore and Mealy FSM.	2	2	5	1
10.	Define Logic Synthesis	2	1	5	1
	Part-B (5×8 = 40 Marks)				
11. a)	Reduce the following Boolean function to minimum literals and draw the logic diagram: (x'y'+z)'+ z + xy + wz.	4	3	1	2
b)	Simplify the following Boolean function using K-map method: $F(A, B, C, D)=\Sigma(0,2,5,7,8,10,11,13,14,15)$	4	3	1	2
12. a)	Explain 4 bit Ripple Carry Adder using neat sketch.	4	2	2	1
b)	Construct 3x8 Decoder using Logic Gates and Truth Table.	4	2	2	1
13. a)	Show the Design of Mod 10 Up Counter (Ripple Counter) using JK Flip Flops and Logic Gates	5	3	3	3
b)	Convert D Flip-Flop to T Flip-Flop.	3	3	3	2
14. a)	Discuss design of 8x1 Multiplexer with suitable Verilog code in gate level modeling	5	2	4	3
b)	Explain any two Compiler directives in Verilog.	3	2	4	1

Contd... 2

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15. a)	Distinguish between Blocking and non Blocking assignment with an example	4	4	5	1
b)	Differentiate between series and parallel blocks.	4	4	5	2
16. a)	Find the complement of the following Boolean function and reduce it to minimum number of literals. (b' d+ a' b c' +a c d+ a' b c)	4	3	1	3
b)	Explain operation of 2 bit Magnitude Comparator with circuit diagram and truth table.	4	2	2	1
17.	Answer any ***two*** of the following:				
a)	Define the following Terms i) Set-up time ii)Hold time iii) Modulo of a counter iv)Shift register	4	1	3	1
b)	Explain continuous assignment statements with delays in data flow modeling.	4	2	4	1
c)	Identify the significance of initial and always blocks	4	4	5	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	40%
iii)	Blooms Taxonomy Level – 3 & 4	40%

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